

Move

Text Search

Close

L3 31 OVERDRIVE AND SEMICONDUCTOR CHIP

=> display

ENTER (L3), L# OR ?:.

ENTER ANSWER NUMBER OR RANGE (1):1-31

ENTER DISPLAY FORMAT (CIT):.

1. 5,550,480, Aug. 27, 1996, Method and means for controlling movement of a chuck in a test apparatus; Randall D. Nelson, et al., 324/754, 756 [IMAGE 10:36:28 COPY AND CLEAR PAGE, PLEASE
03 DEC 96 10:36:37 U.S. Patent & Trademark Office P0008
AVAILABLE]

2. 5,463,335, Oct. 31, 1995, Power up detection circuits; Sridhar Divakaruni, et al., 327/143, 206 [IMAGE AVAILABLE]

3. 5,374,857, Dec. 20, 1994, Circuit for providing drive current to a motor using a sensefet current sensing device and a fast amplifier; Francesco Carobolante, 327/110, 427, 432, 581 [IMAGE AVAILABLE]

4. 5,365,117, Nov. 15, 1994, Logic gates having fast logic signal paths through switchable capacitors; Robert C. Wong, 327/374; 326/14, 18, 52, 89, 126; 327/482 [IMAGE AVAILABLE]

5. 5,357,192, Oct. 18, 1994, Method of contacting a semiconductor die with probes; James C. Van Zee, et al., 324/758, 73.1 [IMAGE AVAILABLE]

6. 5,315,237, May 24, 1994, Touch sensor unit of prober for testing electric circuit and electric circuit testing apparatus using the touch sensor unit; Kenichi Iwakura, et al., 324/754 [IMAGE AVAILABLE]

7. 5,278,432, Jan. 11, 1994, Apparatus for providing radiant energy; Ronald W. Ignatius, et al., 257/88, 99, 723; 327/514; 362/800 [IMAGE AVAILABLE]

8. 5,263,173, Nov. 16, 1993, High speed clocked output driver for switching logic levels of an output pad at integer and integer and a half clock cycles; Craig A. Gleason, 395/800; 307/412; 326/97, 121; 364/932.8, 934.2, 935.42, DIG.2; 395/550 [IMAGE AVAILABLE]

9. 5,198,995, Mar. 30, 1993, Trench-capacitor-one-transistor storage cell and array for dynamic random access memories; Robert H. Dennard, et al., 365/149; 257/301; 365/203 [IMAGE AVAILABLE]

10. 5,173,624, Dec. 22, 1992, Level-shifter circuit for high-speed low-power BiCMOS ECL to CMOS input buffers; Bertrand Gabillard, et al., 326/66, 17, 84, 103 [IMAGE AVAILABLE]

11. 4,943,767, Jul. 24, 1990, Automatic wafer position aligning method for wafer prober; Keiichi Yokota, 324/758; 348/87 [IMAGE AVAILABLE]

12. 4,931,672, Jun. 5, 1990, True TTL to true ECL bi-directional tristatable translator driver circuit; Aurangzeb K. Khan, 326/78, 56, 89, 90 [IMAGE AVAILABLE]

13. 4,868,415, Sep. 19, 1989, Voltage level conversion circuit; William C. Dunn, 327/122, 116, 178, 333 [IMAGE AVAILABLE]

14. 4,860,749, Aug. 29, 1989, Tachycardia detection for automatic implantable cardioverter/defibrillator with atrial and ventricular sensing capability; Michael H. Lehmann, 607/4, 14 [IMAGE AVAILABLE]

15. 4,857,766, Aug. 15, 1989, BiMos input circuit; Wilbur D. Pricer, et al.,

INPUT:

Move

Text Search

Close

16. 4,780,836, Oct. 25, 1988, Method of testing semiconductor devices using a probe card; Tsutomu Miyazaki, et al., 364/551.01; 324/765; 364/550 [IMAGE AVAILABLE]

17. 4,654,826, Mar. 31, 1987, Single device transfer static latch; Roy K. Yamanouchi, et al., 365/189.05, 154 [IMAGE AVAILABLE]

10:36:41 COPY AND CLEAR PAGE, PLEASE

03 DEC 96 10:37:00 U.S. Patent & Trademark Office P0009

18. 4,518,875, May 21, 1985, Three-level MOS logic circuit; Haluk M. Aytac, 326/59, 121 [IMAGE AVAILABLE]

19. 4,513,209, Apr. 23, 1985, Level detector; Kenzo Tanabe, et al., 327/58, 63, 97, 104 [IMAGE AVAILABLE]

20. 4,377,857, Mar. 22, 1983, Electrically erasable programmable read-only memory; Andrew C. Tickle, 365/185.33; 257/321; 365/182, 185.02, 185.06, 185.18, 185.25, 185.26 [IMAGE AVAILABLE]

21. 4,329,705, May 11, 1982, VMOS/Bipolar power switching device; Richard H. Baker, 257/330, 378 [IMAGE AVAILABLE]

22. 4,160,291, Jul. 3, 1979, Precharge circuitry for an electrically alterable non-volatile memory; Philip C. Smith, et al., 365/203; 326/106; 362/184 [IMAGE AVAILABLE]

23. 4,159,540, Jun. 26, 1979, Memory array address buffer with level shifting; Philip C. Smith, et al., 365/189.05; 326/86, 87; 365/230.08 [IMAGE AVAILABLE]

24. 4,137,428, Jan. 30, 1979, Optically actuated bidirectional semiconductor switch; Joseph Federico, et al., 381/123; 307/117; 327/513, 575 [IMAGE AVAILABLE]

25. 4,124,900, Nov. 7, 1978, Memory using interleaved rows to permit closer spacing; Philip C. Smith, et al., 365/72; 326/106; 365/184, 230.08 [IMAGE AVAILABLE]

26. 4,122,401, Oct. 24, 1978, High efficiency power amplifier circuit; Donald Roy Sauer, 330/257, 288, 296, 298 [IMAGE AVAILABLE]

27. 3,922,647, Nov. 25, 1975, External exclusive OR type circuit for inverting cell MOS RAM; Bernard D. Broeker, Jr., 365/189.08; 326/52, 106; 327/51; 365/210 [IMAGE AVAILABLE]

28. 3,906,464, Sep. 16, 1975, External data control preset system for inverting cell random access memory; William Walter Lattin, 365/182, 202 [IMAGE AVAILABLE]

29. 3,906,463, Sep. 16, 1975, MOS memory system; Robert Tapei Yu, 365/182; 326/106; 365/202 [IMAGE AVAILABLE]

30. 3,751,681, Aug. 7, 1973, MEMORY SELECTION APPARATUS; William F. Jordan, Jr., 326/26, 30, 90, 101, 128; 327/579 [IMAGE AVAILABLE]

31. 3,611,170, Oct. 5, 1971, BIAS NETWORKS FOR CLASS B OPERATION OF AN AMPLIFIER; Carl Franklin Wheatley, Jr., 330/266; 327/535; 330/149, 255, 257, 261, 267 [IMAGE AVAILABLE]

=>

INPUT:
